

**REMARKS/ARGUMENTS**

*1. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Himes (Himes et al., US 4,731,696) in view of applicant's admitted prior art ("AAPA")*

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**Response:**

Claim 1 has been amended to overcome the above rejection. Specifically, claim 1 now includes additional limitations regarding a  
10 **second isolation layer covering the capacitor and the substrate and a first contact plug located only in the second isolation layer and electrically connected to the first electrode.** The above limitations originally recited in claims 2 and 3 are included in order to further define the structural considerations given to the claimed invention and no new  
15 matter is introduced.

Himes taught a three plate integrated circuit capacitor comprising a substrate 10, a passivating oxide layer 11, a silicide layer 12', a dielectric oxide 13', and a second silicide plate 15' overlying the oxide layer 13' and  
20 being in turn overcoated with a second oxide layer 16' which is made to duplicate the oxide layer 13'. At this point, via holes 19 and 20 are photolithographically etched as shown in Fig. 7. **The via hole 19 extends through the oxide layer 16' to expose the silicide layer 15'. The via hole 20 extends through the oxide layers 13' and 16' to expose the silicide**  
25 **layer 12' (Figs. 4-7, column 3, lines 27-46).**

It is noteworthy that Himes' oxide layer 13' is entirely deposited on the

substrate, therefore the via hole 20 has to extend through oxide layers 13' and 16' to complete electrical connection with the capacitor plate 12'. In other words, **via hole 20 is located in BOTH oxide layers 13' and 16'.** Contrary to Himes, **the first contact hole of the present application is located ONLY in the second isolation layer and electrically connected to the first electrode.** The applicant believes the present application is distinctly different from Himes' three plate integrated circuit capacitor. Therefore reconsideration of the amended claim 1 is politely requested.

10        Claim 11 has been amended to overcome the above rejection. Specifically, claim 11 now includes additional limitations regarding "an isolation layer covering the first polysilicon layer and the second polysilicon layer and a first contact plug located only in the isolation layer and electrically connected to the first polysilicon layer". The above  
15        limitations are supported by the specification, for instance in Fig.6 and originally recited in claim 12. No new matter is introduced.

As mentioned above, **Himes' oxide layer 13' is entirely deposited on the substrate, therefore the via hole 20 has to extend through oxide**  
20        **layers 13' and 16' to complete electrical connection with the capacitor plate 12'. In other words, via hole 20 is located in BOTH oxide layers 13' and 16'. Contrary to Himes, the first contact hole of the present application is located ONLY in the isolation layer and electrically connected to the first polysilicon layer.** The applicant believes the  
25        present application is distinctly different from Himes' three plate integrated circuit capacitor. Therefore reconsideration of the amended claim 11 is politely requested.

Claims 2-3 and 12 are cancelled and no longer in need of consideration.

Claims 4-5 and 13 are amended to obtain a correct antecedent and no  
5 new matter is introduced.

Claims 4-5 and 13-14 are respectively dependent on claim 1 and 11 and  
should be allowed if claims 1 and 11 are allowed. Reconsideration of  
claims 4 and 13 is therefore requested.  
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Claims 6 and 15 are respectively dependent on claims 5 and 14 and  
should be allowed if claims 5 and 14 are allowed. Reconsideration of  
claims 6 and 15 is therefore requested.

Claims 7 and 16 are respectively dependent on claims 1 and 11 and  
should be allowed if claims 1 and 11 are allowed. Reconsideration of  
claims 7 and 16 is therefore requested.  
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Claims 8-10 are dependent on the amended claim 1 and should be  
20 allowed if the amended claim 1 is allowed. Reconsideration of claims 8-10  
is therefore requested.

Applicant respectfully requests that a timely Notice of Allowance be  
issued in this case.  
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Sincerely yours,

Winston Hsu

Date: 11/23/2006

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- 10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)